101-790.00
102-82.00 (1)
103-44.00 (2)

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PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	93-C-032C3	*Total Pages*	25
First Named Inventor or Application Identifier	Alex Kalnitsky		
Express Mail Label No.	EM044795993US		

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [ ] Specification [*Total Pages* 20] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [*Total Sheets* 4]
4. Oath or Declaration [*Total Pages* 4]
   - a. [ ] Newly executed (original or copy)
   - b. [X] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: Copy of extension of time petition in parent application

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
    [X] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: 08/456,343

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* *or* [X] *Correspondence address below*

NAME	Lisa K. Jorgenson				
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01/15/98 2374 U.S. PTO

FEE TRANSMITTAL

Note: Effective October 1, 1997.
Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 916

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Alex Kalnitsky
Group Art Unit	2503
Examiner Name	S. Meier
Attorney Docket Number	93-C-032C3

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number
Deposit Account Name

☐ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. ☒ Payment Enclosed:
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790

2. CLAIMS

			Extra		Fee from below		Fee Paid
Total Claims	22	-20 =	2	X	22	=	44
Independent Claims	4	- 3 =	1	X	82	=	82
Multiple Dependent Claims				X	270	=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	82	209	41	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 126

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

Typed or Printed Name	Richard A. Bachand	Date		Complete (if applicable) Reg. Number	25,107
Signature	Richard A Bachand	Date	1/15/98	Deposit Account User ID	

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PATENT
Attorney Docket No. 93-C-32C3
Express Mail Label No. EM044795993US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
Alexander Kalnitsky et al.	)	Group Art Unit:
	)	
Serial No.	)	Examiner:
	)	
Filed: HEREWITH	)	
	)	
For: ENHANCED PLANARIZATION TECHNIQUE FOR AN INTEGRATED CIRCUIT	)	

CERTIFICATE OF MAILING BY EXPRESS MAIL

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

The undersigned hereby certifies that the accompanying UTILITY PATENT APPLICATION TRANSMITTAL, FEE TRANSMITTAL, PRELIMINARY AMENDMENT, This Certificate of Mailing by Express Mail, and Return Card, all relating to the above application, were deposited as "Express Mail", Mailing Label No. EM044795993US, with the United States Postal Service, addressed to The Assistant Commissioner for Patents, Washington, D.C. 20231 on January 15, 1998

January 15, 1998 Helen M Schmidt
Date Mailer

1/13/98 Richard A Bachand
Date

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(303) 295-8563

PATENT
Express Mail No. EM044795993US
Attorney Docket No. 93-C-32C3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Alexander Kalnitsky et al.	)	Group Art Unit:
	)	
Serial No.	)	Examiner:
	)	
Filed: HEREWITH	)	
	)	
For: ENHANCED PLANARIZATION TECHNIQUE FOR AN INTEGRATED CIRCUIT	)	

09/456343 06/01/95

PRELIMINARY AMENDMENT

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

This preliminary amendment accompanies a continuation application, filed under 35 U.S.C. §53(b), of parent application serial number 08/456,343, filed June 1, 1995, by the applicant hereof. Said prior application serial number 08/456,343 was under final rejection, and the proposed amendment filed therein was not entered. The contents of said amendment are repeated hereinbelow. Entry is respectfully requested prior to calculation of the issue fee and examination on the merits.

IN THE SPECIFICATION

Please amend the specification as follows:

Page 1, line 1, please insert the following paragraph:

--This application is a continuation of copending patent application serial number 08/456,343, filed June 1, 1995.--

IN THE CLAIMS

Claims 1-25 were in the original application.

Please cancel claims 1, 8, and 15.

Please amend claims 2-7, 9-14, and 16-25 as follows:

Please amend claims 2-7, 9-14, and 16-24 as follows:

2 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said deposition step (c.) is plasma-enhanced.

3 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said deposition step (c.) uses TEOS as a source gas.

4 (Amended). The [method] integrated circuit of Claim [1] 22, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

5 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

6 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

7 (Amended). The [method] integrated circuit of Claim [1] 22, wherein said interlevel dielectric is a doped silicate glass.

9 (Amended). The [method] integrated circuit of Claim [8] 23, wherein said deposition step (c.) is plasma-enhanced.

10 (Amended). The [method] integrated circuit of Claim [8] 23, wherein said deposition step (c.) uses TEOS as a source gas.

11 (Amended). The [method] integrated circuit of Claim [8] 23, comprising the additional step of applying a passivating

dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

12 (Amended). The [method] integrated circuit of Claim [8] 23, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

13 (Amended). The [method] integrated circuit of Claim [8] 23, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

14 (Amended). The [method] integrated circuit of Claim [8] 23, wherein said interlevel dielectric is a doped silicate glass.

16 (Amended). The [method] integrated circuit of Claim [15] 24, wherein said deposition step (c.) is plasma-enhanced.

17 (Amended). The [method] integrated circuit of Claim [15] 24, wherein said deposition step (c.) uses TEOS as a source gas.

18 (Amended). The [method] integrated circuit of Claim [15] 24, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

19 (Amended). The [method] integrated circuit of Claim [15] 24, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

20 (Amended). The [method] integrated circuit of Claim [15] 24, wherein said interlevel dielectric is a doped silicate glass.

21 (Amended). The [method] integrated circuit of Claim [15] 24, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

22 (Amended). An integrated circuit manufactured by the method [of claim 1.] comprising the acts of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer;
(d.) applying and curing spin-on glass, to form a third dielectric layer, to produce a stack including said third dielectric layer over said first and second dielectric layers;
(e.) performing a global etchback to substantially remove portions of said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;
(f.) deposition of an interlevel dielectric at least over said remaining third dielectric layer;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

23 (Amended). An integrated circuit manufactured by the method [of claim 8.] comprising the acts of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing silicon dioxide, to form a second dielectric layer over said first dielectric layer;
(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second layers;
(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated

structure, wherein at least a portion of said spin-on glass of said third dielectric layer remains after said global etchback;
(f.) deposition of an interlevel dielectric at least over said remaining spin-on glass of said third dielectric layer;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

24 (Amended). An integrated circuit manufactured by the method [of claim 15.] comprising the acts of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer, said second dielectric layer having a thickness equal to or less than said first dielectric layer;
(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second dielectric layers, said third dielectric layer having a thickness equal to or greater than said second layer;
(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;
(f.) deposition of an interlevel dielectric at least over said remaining second dielectric layer;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

Claim 25, line 17, change "selectred" to --selected--.

REMARKS

Claims 22, 23, and 24, have been amended from the parent application in several respects. The first, which was not necessitated by the examiner's rejection, is to make them independent so that claims 2-7, 9-14, and 16-21 may depend respectively therefrom. The second is to clarify the language of the dielectric layers to distinguish from dielectric materials in some recitations and dielectric layers in others. The third is to clarify the identity of the third layer which is only partially removed, to leave remaining a portion of SOG over an interlevel dielectric of the second layer. The claims originally presented erroneously referred to the removal only of the second layer without reference to the removal of the third, and in which a portion of the third dielectric layer remained after global etchback. The fourth change made to the claims, also not necessitated by the examiner's rejection is to claim the steps of the method as "acts", in accordance with the language permitted by the sixth paragraph of 35 U.S.C. §112.

Claim groups 2-7, 9-14, and 16-21 have been amended to depend respectively from now independent claims 22, 23, and 24.

Claim 25 has been amended to correct a typographical error on line 17.

THE PRIOR 35 U.S.C. §103 REJECTION

Claims 2-7, 9-14, and 16-25, had been rejected in the parent application under 35 U.S.C. §103(a) as being obvious from Elkins (4,676,867).

In the parent application, the examiner apparently misunderstood the arguments made in distinguishing the structure that results from the process advanced in the Amendment filed September 15, 1997. Apparently, the examiner was of the opinion that the arguments were directed toward the novelty of the

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process, rather than the novelty of the resulting structure. However, it appears that no consideration had been given to the distinctions between the resulting structure and the structure of Elkins that were advanced in the September 15, 1997, Amendment. Specifically, and with respect to the claims themselves, the resulting structure includes a first dielectric formed of SOG, a second dielectric over the SOG, a third dielectric layer formed of SOG over the first and second dielectric layers, forming a dielectric stack that contains at least portions of all three dielectric layers after planarization. This is in clear distinction to the structure of Elkins, et al., which includes only a single SOG layer 24.

The invention is not obvious in view of the Elkins, et al. reference since there is no hint or suggestion of a dielectric stack that includes top and bottom SOG materials with an interlevel dielectric therebetween. The advantages of such a structure having a lower SOG dielectric layer are outlined in the application and in the previously filed Amendment of September 15, 1997. The top layer of SOG also results in the advantage of enabling better planarization to be effected, lowering the risk of cracking.

Thus, it is respectfully submitted that the claimed invention is not obvious from the Elkins, et al. reference. Rejection should be withdrawn and the claims should be allowed.

CONCLUSION

As above pointed out, claims 2-7, 9-14, and 16-25, are patentable over Elkins. It is therefore respectively requested that all of said claims be allowed and the case be advanced to issue.

Respectfully submitted,

Richard A. Bachand

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January 13, 1998

09007668.041598

Enhanced Planarization Technique for an Integrated Circuit

U.S. Patent Application of:

Alex Kalnitsky, Inventor
Yih-Shung Lin, Inventor

SGS-Thomson Microelectronics, Inc., Assignee

Attorney's Docket No. SGS-011/93-C-32
Robert Groover, REG.PAT.ATTY.

Background and Summary of the Invention

The present invention relates to formation and structures for interlevel dielectrics in integrated circuit fabrication.

A high degree of planarization is essential in the fabrication of integrated circuits with multiple levels of interconnect. Application of spin-on glass,[1] followed by global etch-back, is widely used in the industry to achieve the desired level of surface planarity. However, spin on glass ("SOG") and SOG etch-back technique are inadequate in a variety of situations where topologies with high aspect ratio and/or more topologies are encountered due to lack of planarization and/or sog cracks.

In most cases, successful planarization of severe topologies is achieved by a single or double SOG deposition+etchback step in the following sequence:

a) a layer of dielectric is applied between the underlying surface and SOG.

b) application of a layer of SOG and SOG cure;

---

[1]Spin-on glass deposition is an example of a "sol-gel" process, which has been used in the semiconductor industry for many years. The unprocessed spin-on glass material (available in numerous formulations) is a fluid material (actually a gel). After the liquid material is coated onto the face of a wafer, the wafer is rotated at high speed to throw off the excess material. The surface tension and adhesion of the material provides a flat (planarized) surface with a controlled thickness. The liquid material is then baked, to drive off solvents and provide a stable solid silicate glass. *See generally, e.g.*, Dauksher *et al.*, "Three 'low Dt' options for planarizing the pre-metal dielectric on an advanced double poly BiCMOS process," 139 J.ELECTROCHEM.SOC. 532-6 (1992), which is hereby incorporated by reference.

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c) application of a second layer of SOG and SOG cure (optional); and
d) SOG etchback.

However, in extreme topologies, when the volume of SOG is very large, shrinkage of SOG during planarization and post-planarization processing leads to formation of undesirable cracks or voids.

The proposed method seeks to alleviate the problem of SOG cracking by performing the following operations:

a) Conventional dielectric deposition is applied (optional);
b) Application of a layer of SOG and SOG cure (as in prior art);
c) deposition of a layer of dielectric (e.g. TEOS/ozone deposition, or simple plasma-enhanced-TEOS,[2] or plasma-enhanced-silane oxide) with or without dopant can be used to adjust for etch back selectivity between SOG and dielectric. Thicknesses between 1000Å to 5000Å can be used.
d) application of a second layer of SOG and/or SOG cure: and
e) SOG etchback.

This process will leave a layer of dielectric between the 1st and the 2nd SOG layers in locations where conventional planarization technique are likely to crack or void. This provides enhanced reliability.

The thickness of the first SOG layer can be reduced to avoid any undesired effects, such as field inversion of underlying devices or

[2]"TEOS," or tetraethoxysilane, is a popular and convenient feedstock for deposition of oxides from the vapor phase.

enhanced hot-carrier injection.[3]

A positive sloped valley is produced for second dielectric deposition. The step coverage will be enhanced due to this positive slope.

The structure provided by these steps has improved resistance to cracking, and improved resistance to other undesirable possible effects of thick spin-on glass layers.

According to a disclosed class of innovative embodiments, there is provided: An integrated circuit fabrication method, comprising the steps of: providing a partially fabricated integrated circuit structure; applying and curing spin-on glass, to form a first dielectric; depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer; applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers; performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure; deposition of an interlevel dielectric; etching holes in said interlevel dielectric in predetermined locations; and depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

According to a disclosed class of innovative embodiments, there is provided: An integrated circuit fabrication method, comprising the steps of: providing a partially fabricated integrated circuit structure;

[3]*See, e.g.*, Lifshitz *et al.*, "Hot-carrier aging of the MOS transistor in the presence of spin-on glass as the interlevel dielectric," 12 IEEE ELECTRON DEVICE LETTERS 140-2 (March 1991), which is hereby incorporated by reference.

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applying and curing spin-on glass, to form a first dielectric; depositing silicon dioxide under vacuum conditions, to form a second dielectric layer over said first layer; applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers; performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure; deposition of an interlevel dielectric; etching holes in said interlevel dielectric in predetermined locations; and depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

According to a disclosed class of innovative embodiments, there is provided: An integrated circuit fabrication method, comprising the steps of: providing a partially fabricated integrated circuit structure; applying and curing spin-on glass, to form a first dielectric layer; depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer, said second dielectric layer having a thickness equal to or less than said first layer; applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers, said third dielectric layer having a thickness equal to or greater than said second layer; performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure; deposition of an interlevel dielectric; etching holes in said interlevel dielectric in predetermined locations; and depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

According to a disclosed class of innovative embodiments, there

is provided: An integrated circuit, comprising: an active device structure, including therein a substrate, active device structures, isolation structures, and one or more patterned thin film conductor layers including an uppermost conductor layer; and a planarization structure, overlying recessed portions of said active device structure, comprising a layer of sol-gel-deposited dielectric overlain by a layer of vacuum-deposited dielectric overlain by a further layer of sol-gel-deposited dielectric; an interlevel dielectric overlying said planarization structure and said active device structure, and having via holes therein which extend to selected locations of said uppermost conductor layer; and an additional thin-film patterned conductor layer which overlies said interlevel dielectric and extends through said via holes to said selectred locations of said uppermost conductor layer.

Brief Description of the Drawing

The present invention will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

Figures 1A-1C show steps in a conventional process;

Figures 2A-2C show steps in a first embodiment of the invention;

Figures 3A-3C show steps in a second embodiment of the invention.

Figure 4 shows a sample device structure incorporating a planarization layer according to the disclosed innovations.

Description of the Preferred Embodiments

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit <u>any</u> of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

The disclosed process steps can be applied, for example, after fabrication of the first metal layer. Thus, the starting structure would be patterned metallization lines running over an interlevel dielectric which includes contact holes, and also has topographical excursions due to the underlying polysilicon layer(s) and field oxide layer. The maximum topographical excursion will include contributions from all of these. (However, the disclosed innovations can also be applied after fabrication of the second metal layer, before deposition of a third metal layer.)

Figures 1A-1C show steps in a conventional process. The starting structure will of course be defined by the previous process steps; but assume, for example, that the recesses have widths of 0.8 μm each, are spaced on a minimum pitch of 1.6 μm, and have a maximum depth of 1 μm. (Of course, these numbers are merely illustrative.)

As shown in Figure 1A, a first layer 1 of SOG would be spun on and cured, to a thickness of e.g. 3000Å in flat areas. (The thickness is substantially more in recessed areas.) As is well known to those of

ordinary skill, the thickness of the SOG is determined by the individual composition and by the spin rate. As seen in Figure 1A, a single deposition of SOG is not enough to fill the recesses.

As shown in Figure 1B, a second layer 2 of SOG would then be spun on and cured, to provide an additional thickness of e.g. 3000Å in flat areas.

A global etchback step is then performed, to remove the SOG from flat areas. The resulting surface contour, as shown in Figure 1C, is susceptible to cracking.

Figures 2A-2C show steps in a first embodiment of the invention. Assume that the same recess dimensions are used as in Figures 1A-1C. Again, the specific dimensions and parameters given here are merely illustrative, and do not delimit the invention.

A first layer 1 of SOG is deposited as in Figure 1A. That is, for example, a siloxane-based spin-on glass[4] is spun on to a thickness of 2000Å over flat areas, and is then cured for 60 minutes at 425°C.

A layer 3 of low-temperature oxide is then deposited, to a thickness of 2000Å. (For example, this may be done by plasma-enhanced deposition of TEOS.) This produces the structure shown in Figure 2B.

A second layer 2 of SOG is then be spun on and cured, to provide an additional thickness of e.g. 3000Å in flat areas.

A global etchback step is then performed, to remove the SOG and TEOS from flat areas. The resulting surface contour, as shown in

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[4]Such materials may be obtained, for example, from Ohka America™ or Allied Signal™ or other suppliers.

Figure 2C, provides improved filling of the recessed areas. Moreover, the combination of slightly different materials (SOG and low-temperature oxide) reduces susceptibility to cracking.

For simplicity, the drawing of Figure 2C shows exactly 100% etchback, but of course the degree of etchback can be varied if desired.

Figures 3A-3C show steps in a second embodiment of the invention. This may be particularly advantageous with more extreme topologies. In this embodiment, assume, for example, that the recessed areas have widths of 0.8 μm each, are spaced on a minimum pitch of 1.6 μm, and have a maximum depth of 2 μm. (Of course, these numbers are merely illustrative.)

A first layer 1 of SOG is spun on and cured to produce a thickness of 2000Å over flat areas, as shown in Figure 3A.

A layer 3 of low-temperature oxide is then deposited, to a thickness of 3000Å. (For example, this may be done by plasma-enhanced deposition of TEOS.) This produces the structure shown in Figure 3B.

A second layer 2 of SOG is then be spun on and cured, to provide an additional thickness of e.g. 2000Å in flat areas.

A global etchback step is then performed, to remove the SOG and TEOS from flat areas. The resulting surface contour, as shown in Figure 3C, provides improved filling of the recessed areas, even under extreme topologies. Moreover, the combination of slightly different materials (SOG and low-temperature oxide) reduces susceptibility to cracking.

For simplicity, the drawing of Figure 3C shows exactly 100% etchback, but of course the degree of etchback can be varied if desired.

In alternative embodiments, it is also possible to deposit a plasma oxide before the first layer of spin-on glass. (This is commonly done to prevent direct contact between the SOG and the underlying metallization.) In this embodiment, 1000Å-5000Å of (for example) TEOS oxide would be deposited before the first layer of SOG.

Processing then continues with deposition of an interlevel dielectric, such as PSG, and conventional further processing steps.

One particular advantage of the disclosed invention is that it can be very easily implemented (in at least some processes) by a simple transposition of steps (depositing the low-temperature oxide before, rather than after, the second layer of spin-on glass).

Figure 4 shows a sample device structure incorporating a planarization layer according to the disclosed innovations. In this example, the partially fabricated device structure included active devices 12 in a substrate 10, including polysilicon lines 14. Field oxide 13 provides lateral separation active devices. Metal lines 18 overlie a first interlevel dielectric 16 (e.g. of BPSG over TEOS), and make contact to active device areas at contact locations 20. (This provides the starting structure on which planarization is performed as described above.) A planarization layer 22 is then deposited, by the techniques described above, to reduce or eliminate the topographical excursions of the structure. An interlevel dielectric 24 overlies the planarization layer 22 (and the rest of the planarized structure), and includes via holes 25 through which a second metal layer 26 contacts the first metal layer 18. The structure shown can be topped by a protective overcoat (not shown) through which holes are etched to expose locations of contact pads in the second metal layer.

Further Modifications and Variations

It will be recognized by those skilled in the art that the innovative concepts disclosed in the present application can be applied in a wide variety of contexts. Moreover, the preferred implementation can be modified in a tremendous variety of ways. Accordingly, it should be understood that the modifications and variations suggested below and above are merely illustrative. These examples may help to show some of the scope of the inventive concepts, but these examples do not nearly exhaust the full scope of variations in the disclosed novel concepts.

The disclosed innovative steps have been described in the context of via formation (e.g. forming connections from second metal to first metal, or third metal to second metal). Due to the accumulated topographical excursions, planarization is especially desirable at these stages. However, the disclosed innovative concepts can also be applied to planarization of lower levels as well.

The disclosed innovative concepts can also be applied to other spin-on materials, such as polyimide or polymethylmethacrylate.

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given.

CLAIMS

What is claimed is:

1. An integrated circuit fabrication method, comprising the steps of:
   (a.) providing a partially fabricated integrated circuit structure;
   (b.) applying and curing spin-on glass, to form a first dielectric;
   (c.) depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer;
   (d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers;
   (e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure;
   (f.) deposition of an interlevel dielectric;
   (g.) etching holes in said interlevel dielectric in predetermined locations; and
   (h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

2. The method of Claim 1, wherein said deposition step (c.) is plasma-enhanced.

3. The method of Claim 1, wherein said deposition step (c.) uses TEOS as a source gas.

4. The method of Claim 1, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

5. The method of Claim 1, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

6. The method of Claim 1, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

7. The method of Claim 1, wherein said interlevel dielectric is a doped silicate glass.

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8. An integrated circuit fabrication method, comprising the steps of:
   (a.) providing a partially fabricated integrated circuit structure;
   (b.) applying and curing spin-on glass, to form a first dielectric;
   (c.) depositing silicon dioxide under vacuum conditions, to form a second dielectric layer over said first layer;
   (d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers;
   (e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure;
   (f.) deposition of an interlevel dielectric;
   (g.) etching holes in said interlevel dielectric in predetermined locations; and
   (h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

9. The method of Claim 8, wherein said deposition step (c.) is plasma-enhanced.

10. The method of Claim 8, wherein said deposition step (c.) uses TEOS as a source gas.

11. The method of Claim 8, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

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12. The method of Claim 8, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

13. The method of Claim 8, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

14. The method of Claim 8, wherein said interlevel dielectric is a doped silicate glass.

15. An integrated circuit fabrication method, comprising the steps of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer, said second dielectric layer having a thickness equal to or less than said first layer;
(d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers, said third dielectric layer having a thickness equal to or greater than said second layer;
(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure;
(f.) deposition of an interlevel dielectric;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

16. The method of Claim 15, wherein said deposition step (c.) is plasma-enhanced.

17. The method of Claim 15, wherein said deposition step (c.) uses TEOS as a source gas.

18. The method of Claim 15, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

19. The method of Claim 15, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

20. The method of Claim 15, wherein said interlevel dielectric is a doped silicate glass.

21. The method of Claim 15, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

22. An integrated circuit manufactured by the method of Claim 1.

23. An integrated circuit manufactured by the method of Claim 8.

24. An integrated circuit manufactured by the method of Claim 15.

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25. An integrated circuit, comprising:

(a.) an **active device structure,** including therein a substrate, active device structures, isolation structures, and one or more patterned thin film conductor layers including an uppermost conductor layer; and

(b.) a **planarization structure,** overlying recessed portions of said active device structure, comprising a layer of sol-gel-deposited dielectric overlain by a layer of vacuum-deposited dielectric overlain by a further layer of sol-gel-deposited dielectric;

(c.) an **interlevel dielectric** overlying said planarization structure and said active device structure, and having **via holes** therein which extend to selected locations of said uppermost conductor layer; and

(d.) an **additional thin-film patterned conductor** layer which overlies said interlevel dielectric and extends through said via holes to said selectred locations of said uppermost conductor layer.

ABSTRACT

A method for planarizing integrated circuit topographies, wherein, after a first layer of spin-on glass is deposited, a layer of low-temperature oxide is deposited before a second layer of spin-on glass.

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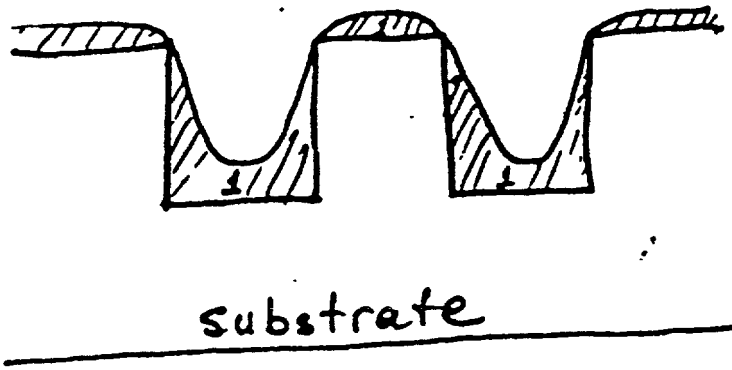
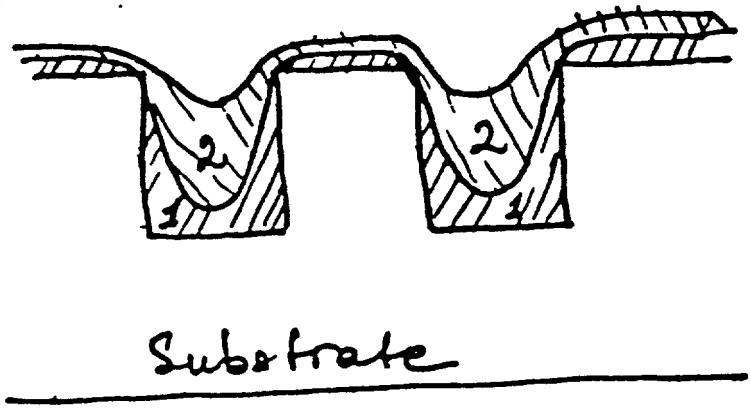


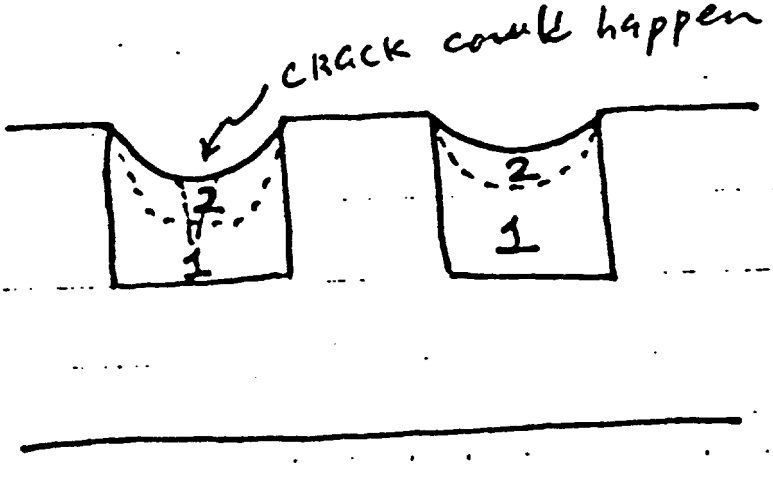
Spin/Cure of SOG-1

Fig. 1A



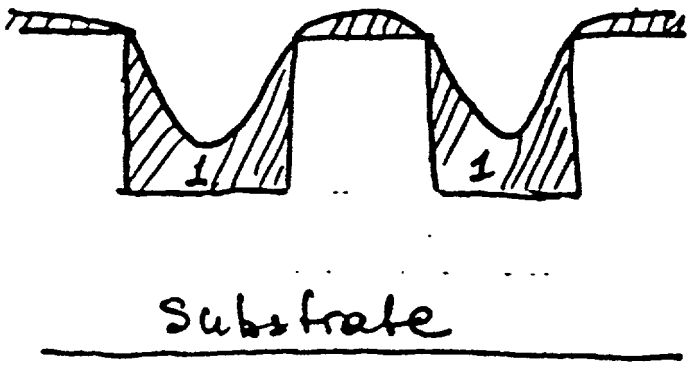
Spin SOG-2
on top of SOG-1
and cure

Fig. 1B



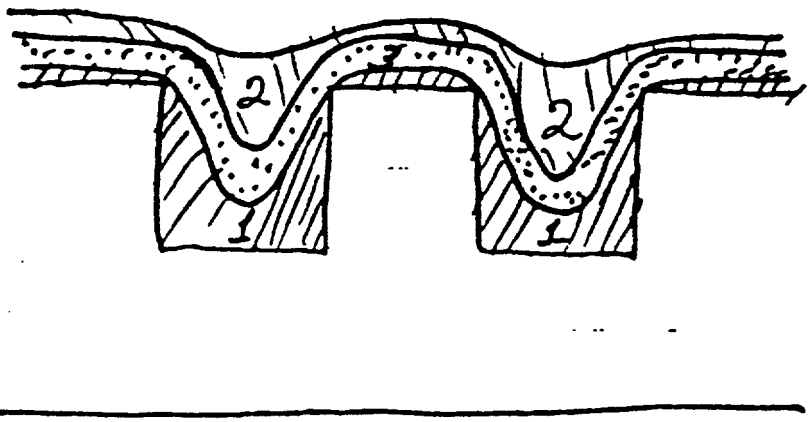
SOG etchback

Fig. 1C



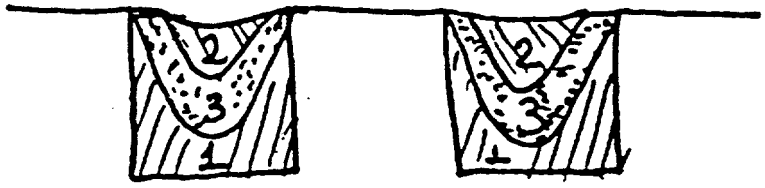
SOG-1 Spin/Cure

Fig. 2A



LTO deposition
and SOG-2 spin cure

Fig. 2B



SOG/LTO etchback

Fig. 2C

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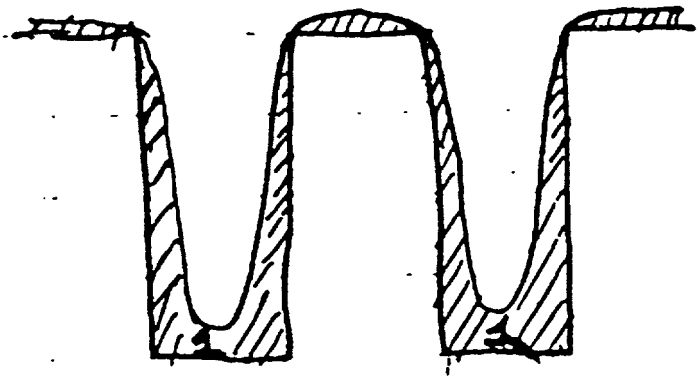
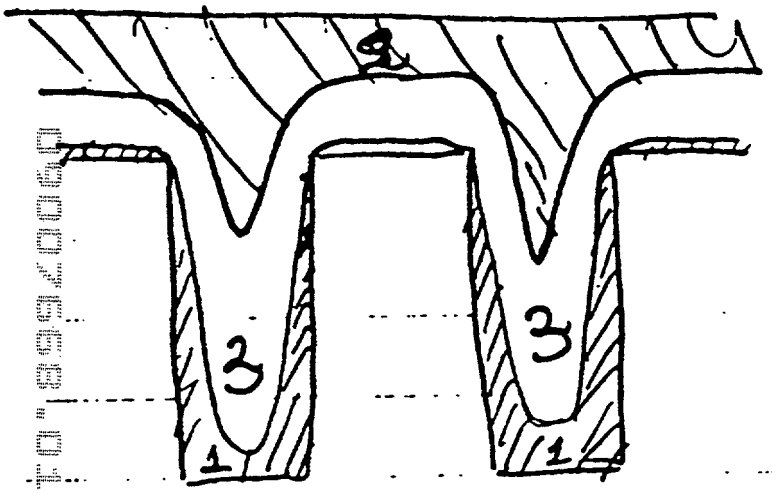


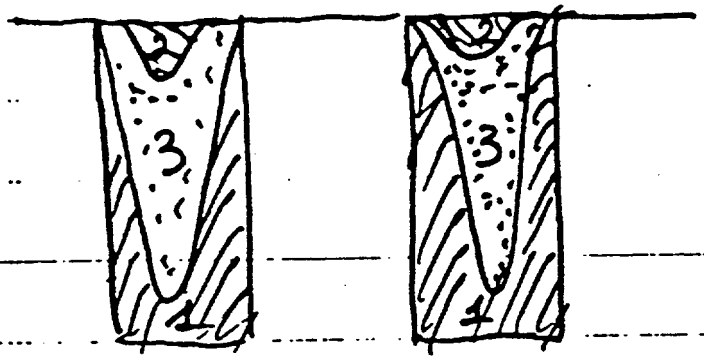
SOG-1 spin/cure

Fig. 3A



LTO deposition and
SOG-2 spin/cure

Fig. 3B



SOG etchback

Fig. 3C

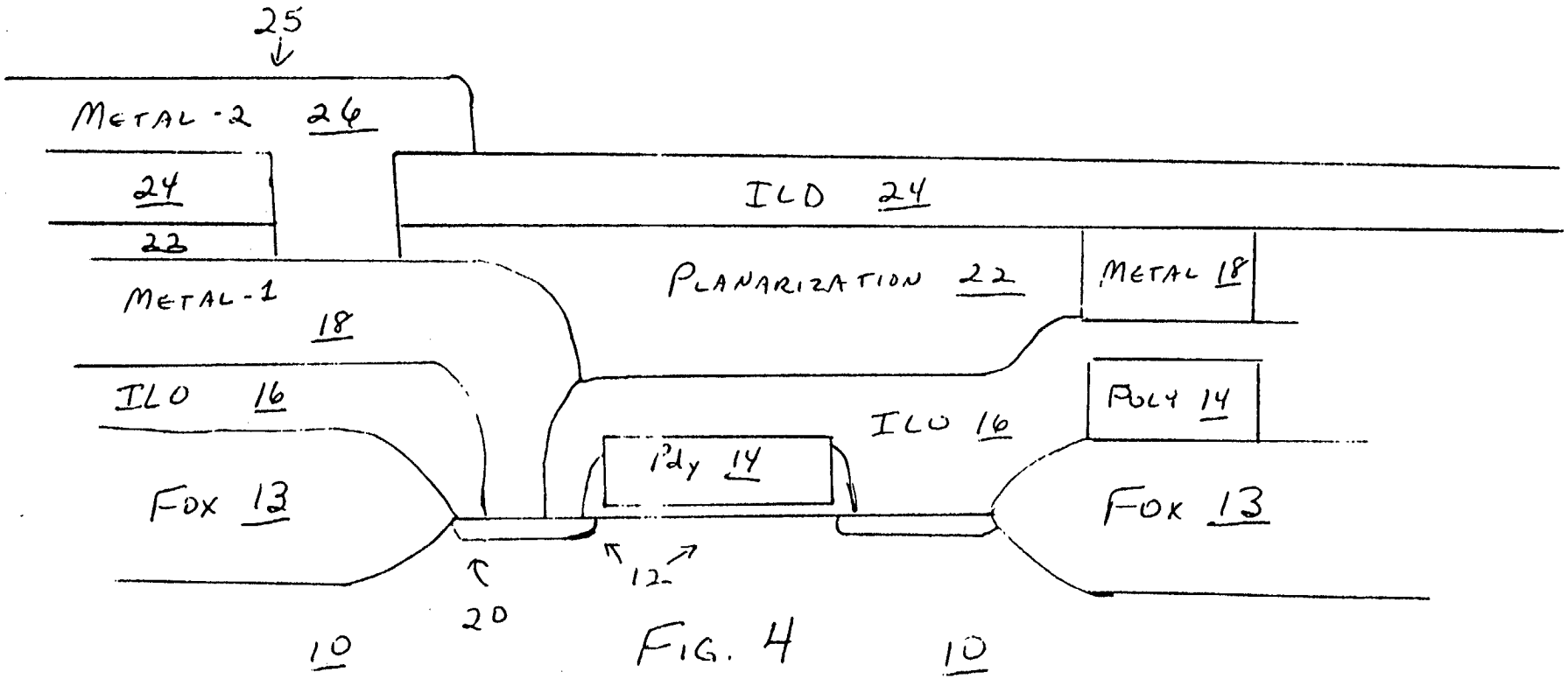

25
METAL-2 26
24
ILD 24
23
METAL-1
18
PLANARIZATION 22
METAL 18
ILD 16
POLY 14
ILD 16
POLY 14
FOX 13
FOX 13
12
20
10
10

FIG. 4

DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below.

I believe that I am an original, first and joint inventor of the innovative subject matter described and claimed in the U.S. patent application, entitled **Enhanced Planarization Technique for an Integrated Circuit** (Att'y Docket No. SGS-011), which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified U.S. patent application, INCLUDING THE CLAIMS.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulation, §1.56(a).

I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention or discovery thereof.

I do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country before my invention or discovery thereof.

I do not know and do not believe that the claimed invention was ever patented or made the subject of an inventor's certificate issued prior to the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns.

I do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country more than one year prior to the filing date of this U.S. application.

I do not know and do not believe that the claimed invention was ever in public use or on sale in the United States of America more than one year prior to the filing date of this U.S. application.

I hereby appoint Robert Groover, Reg.No.30,059, Richard A. Bachand, Reg.No.25,107, Lisa Jorgenson, Reg.No.34,845, and Betty Formby, Reg.No.36,536, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith, and also to file and prosecute any corresponding application in any foreign country.

I hereby direct that all correspondence and telephone calls be addressed to:

Lisa Jorgenson
LEGAL Dept.
SGS-Thomson Microelectronics Inc.
1310 Electronics Drive,
Carrollton TX 75006

(214) 466-7414.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may also jeopardize the validity of the application or any patent issued thereon.

Inventor: Alex Kalnitsky
Date: _____ Signature: _____
Residence and Mailing Address: _____
Citizenship: _____

Inventor: Yih-Shung Lin
Date: 11/30/93 Signature: Yih-Shung Lin
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Citizenship: Republic of China

SGS-THOMSON 000056

DECLARATION AND POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below.

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I hereby direct that all correspondence and telephone calls be addressed to:

Docket No. SGS-011

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